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SIS SCIENCES INGÉNIERIE SANTÉ UNIVERSITÉ DE LYON
ÉCOLE DOCTORALE 488

Assessing BBICS Efficiency in Monitoring Triple-Well Logic and Picosecond LFI

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Application of a physical stress in order to provoke and exploit a malfunction of a system

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Bulk-Built in Current Sensor (BBICS) as a LFI countermeasure [1]

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OUTLINE

- BBICS Principle
- BBICS Experimental State-of-the-Art
- Experimental Methodology & Setup
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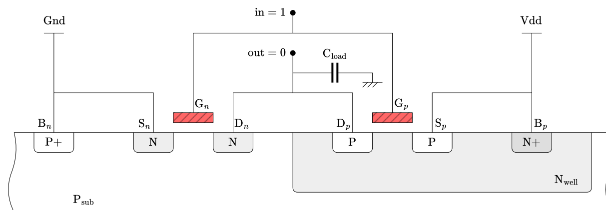
LFI MECHANISM



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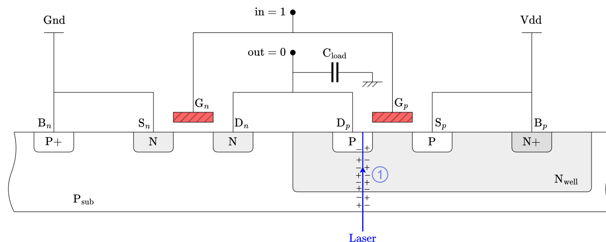

1. Charge Generation (excess charge carriers due to photon absorption)

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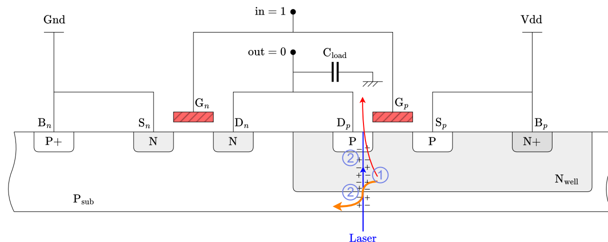

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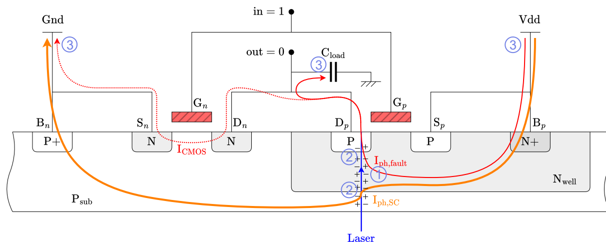

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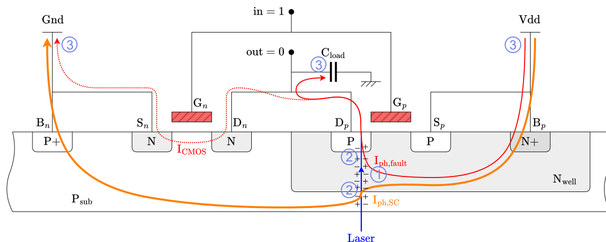
2. Charge Collection (photocurrent generation at PN junctions depletion region)
3. Charge Capture (photocurrents' effect on circuit state)

LFI MECHANISM



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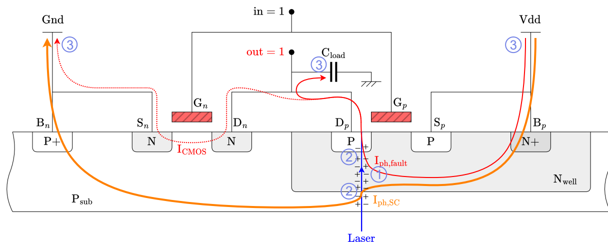

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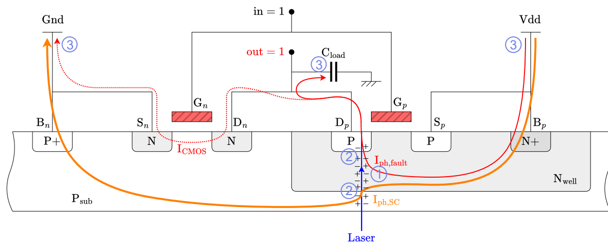

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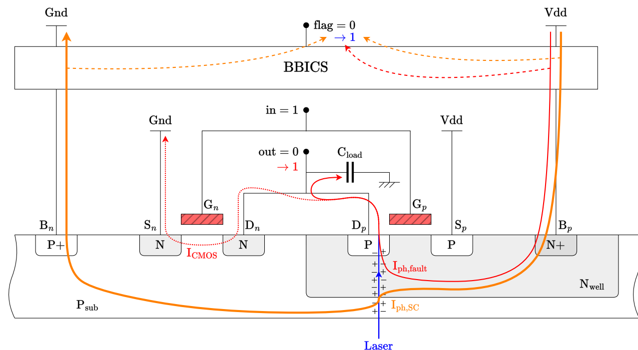
Charges are captured by bulks biasing contacts (B_n and B_p)

MONITORING A DUAL-WELL INVERTER WITH A BBICS



Bulk Built-In Current Sensor (BBICS) monitors abnormal bulk currents

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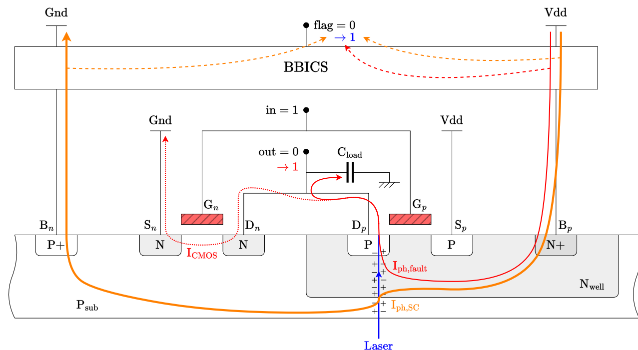

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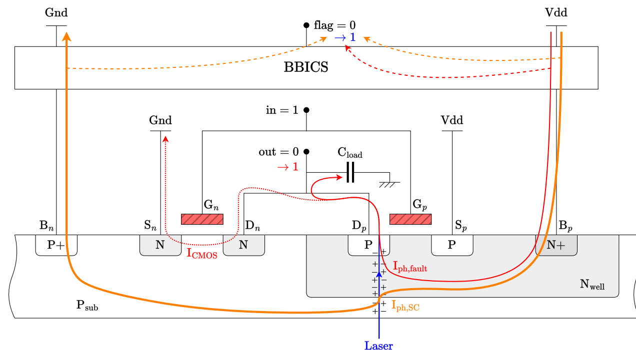
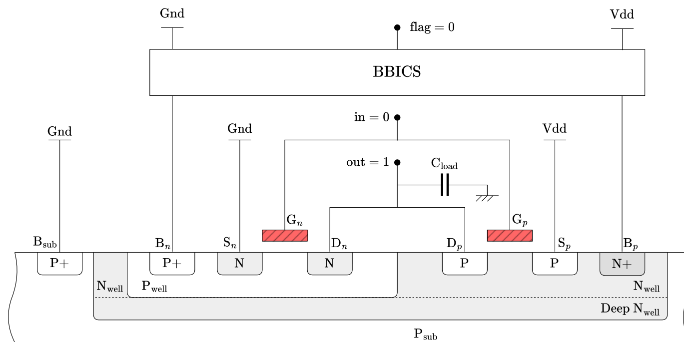


Bulk Built-In Current Sensor (BBICS) monitors abnormal bulk currents

Provides biasing to bulk to ensure photocurrent capture

$I_{ph,SC}$ participates in the detection process

MONITORING A TRIPLE-WELL INVERTER WITH A BBICS



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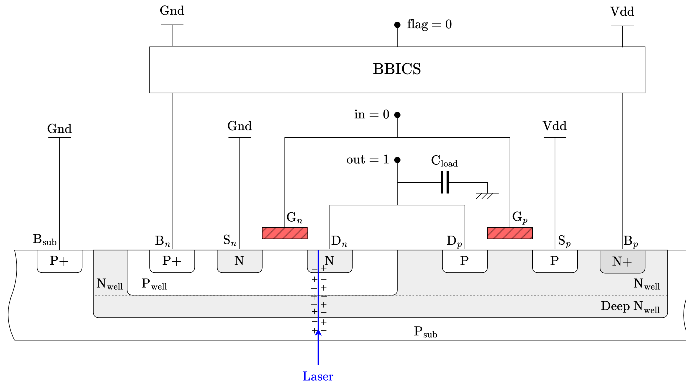

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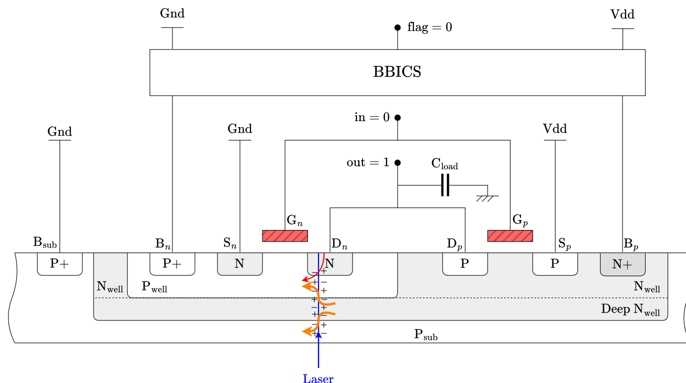

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MONITORING A TRIPLE-WELL INVERTER WITH A BBICS

Gnd
flag = 0
Vdd
BBICS
in = 0
Gnd
Gnd
Vdd
out = 1
C_{load}
$I_{ph,fault}$
G_n
G_p
B_{sub}
B_n
S_n
D_n
D_p
S_p
B_p
P+
P+
N
N
P
P
N+
I_{CMOS}
N_{well}
P_{well}
$I_{ph,SC,1}$
N_{well}
Deep N_{well}
$I_{ph,SC,2}$
P_{sub}
Laser

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→ 1

Vdd

BBICS

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Gnd

Gnd

Vdd

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C_{load}

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G_n

G_p

B_{sub}

B_n

S_n

D_n

D_p

S_p

B_p

P+

P+

N

N

P

P

N+

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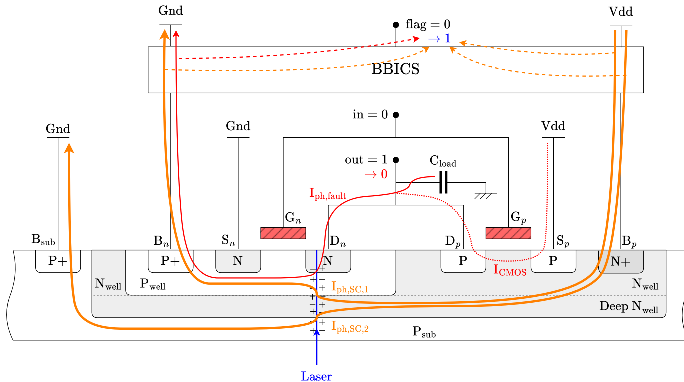

Triple-Well Logic Target ⇒ $I_{SC,1}$ AND $I_{SC,2}$

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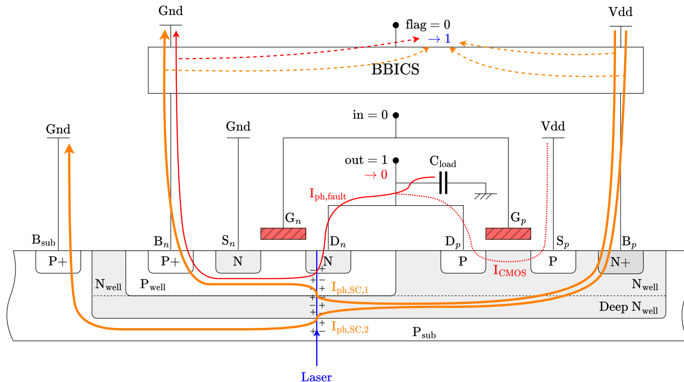

Triple-Well Logic Target ⇒ $I_{SC,1}$ AND $I_{SC,2}$

⇒ Improved (simulated) sensitivity [1]

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MODELING

Accurate modeling is complex:

- Photocurrent generation
- Propagation of photocurrents to the sensor (through bulk)
  - Bulk electrical properties (filtering)
  - Multiple “concurrent” biasing contacts (current divider)
- Other Effects
  - Parasitic bipolar effects (due to bulk potential disruption)
  - IR drop (due to intensive current calls)

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We NEED experimental results !

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STATE-OF-THE-ART

Reference	Champeix *et al.* [1]	Borrel *et al.* [2]	Matsuda *et al.* [3]
Technology	90 nm	90 nm	180 nm
Target	Dual-Well logic	Dual-Well logic Triple-Well logic	Dual-Well AES core
Laser pulse duration	200-50 ns	long μs to short ns	60 ns

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Reference	Champeix *et al.* [1]	Borrel *et al.* [2]	Matsuda *et al.* [3]	**This Work**
Technology	90 nm	90 nm	180 nm	**65 nm**
Target	Dual-Well logic	Dual-Well logic Triple-Well logic	Dual-Well AES core	Dual-Well logic Triple-Well logic
Laser pulse duration	200-50 ns	long μs to short ns	60 ns	50 ns and **30 ps**

Our Contributions:

- Testing for a 65 nm CMOS technology target
- Extend results to picosecond-range pulse testing for standard-cell targets
- Provide additional results on Triple-Well monitoring

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(for “every” : spot position, spot diameter, pulse duration)

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- Ensure (at fault threshold) :

Target area $\subset$ BBICS detection area

SETUP

Backside LFI:

- 120 μm substrate thinning

Laser pulses:

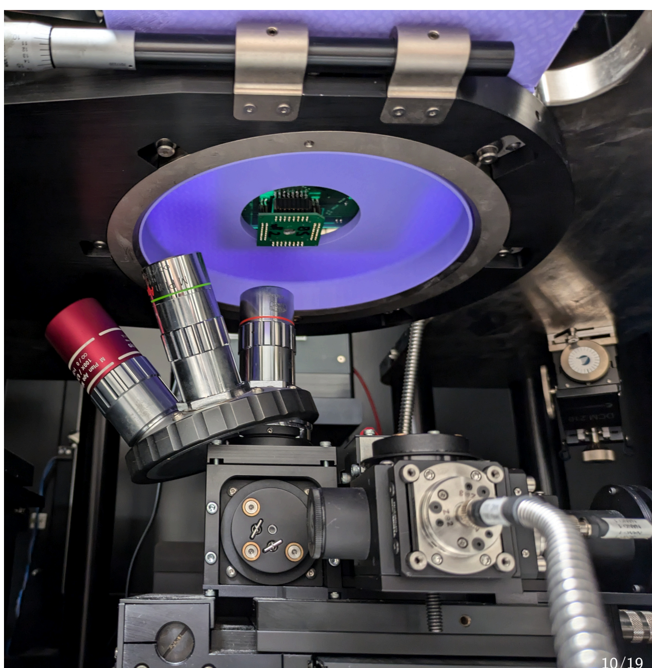
- 50 ns (λ =1,064 nm)
- 30 ps (λ =1,030 nm)

Spot diameters:

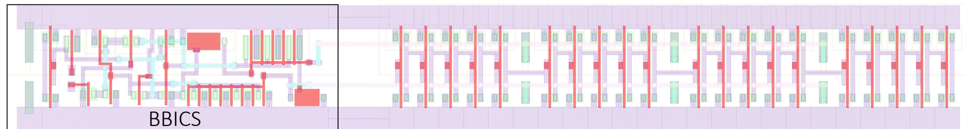
- 5 μm ($\times$20 magnification)
- 1 μm ($\times$100 magnification)

Two test structures...

- 65 nm CMOS technology



DUAL-WELL TEST STRUCTURE



Dual-Well BBICS monitoring a chain of 20 Dual-Well inverters (6 biasing contacts):

- Sensor area : 22 μm^2
- Target area : 40 μm^2

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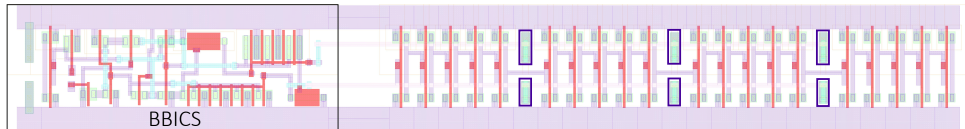

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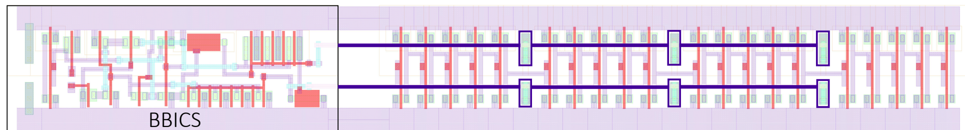

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- Sensor area : $22\,\mu m^2$
- Target area : $40\,\mu m^2$

TRIPLE-WELL TEST STRUCTURE

Pwell

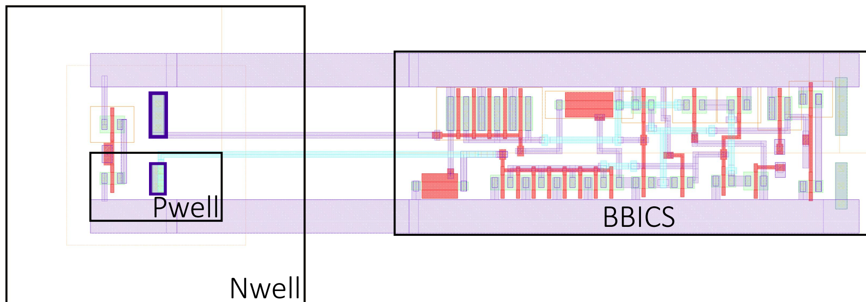
Nwell

BBICS

Dual-Well BBICS monitoring a single Triple-Well inverter (2 biasing contact):

- Sensor area : 22 μm^2
- Target area : 25 μm^2

TRIPLE-WELL TEST STRUCTURE



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- Target area : 25 μm^2

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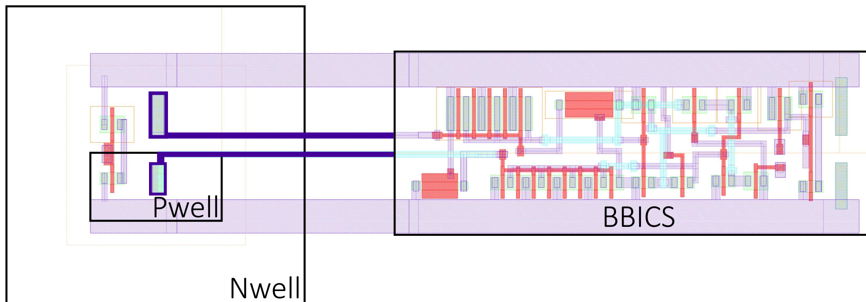

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FAULT THRESHOLDS

Dual-Well fault thresholds (empirical)

Cell	DFF				buffer			
Pulse duration	50ns		30ps		50ns		30ps	
Spot diameter	5 μm	1 μm	5 μm	1 μm	5 μm	1 μm	5 μm	1 μm
Fault threshold	1.9 W	1.7 W	5 nJ	2 nJ	2.1 W	-	5 nJ	3 nJ

FAULT THRESHOLDS

Dual-Well fault thresholds (empirical)

Cell	DFF				buffer			
Pulse duration	50ns		30ps		50ns		30ps	
Spot diameter	5 μm	1 μm	5 μm	1 μm	5 μm	1 μm	5 μm	1 μm
Fault threshold	1.9 W	**1.7 W**	5 nJ	**2 nJ**	2.1 W	-	5 nJ	3 nJ

FAULT THRESHOLDS

Dual-Well fault thresholds (empirical)

Cell	DFF				buffer			
Pulse duration	50ns		30ps		50ns		30ps	
Spot diameter	5 μm	1 μm	5 μm	1 μm	5 μm	1 μm	5 μm	1 μm
Fault threshold	1.9 W	**1.7 W**	5 nJ	**2 nJ**	2.1 W	-	5 nJ	3 nJ

0.85 W **1 nJ**

$$\text{Triple-Well fault threshold} \simeq \frac{\text{Dual-Well fault threshold}}{2}$$

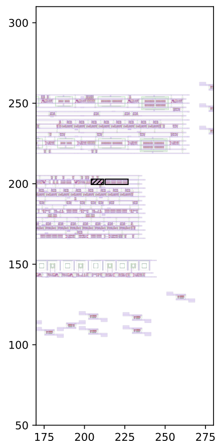
(Borrel *et al.*)

Dual-Well Test Structure : 50 ns pulse, 5 μm spot

Y position (μm)

X position (μm)

Target BBICS Detection

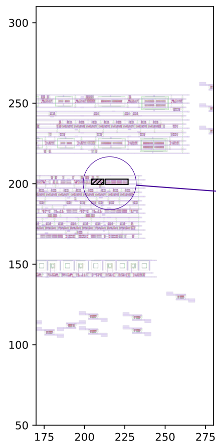


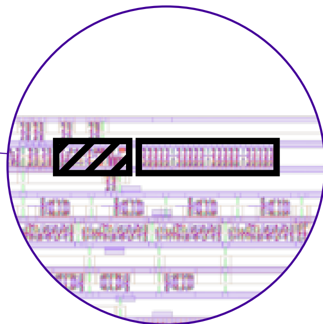
Dual-Well Test Structure : 50 ns pulse, 5 μm spot

Y position (μm)

X position (μm)

Target BBICS Detection



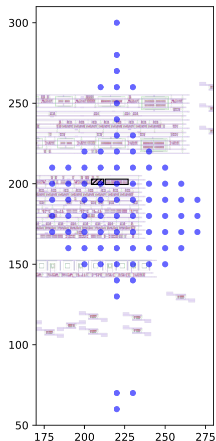


Dual-Well Test Structure : 50 ns pulse, 5 μm spot

Y position (μm)

X position (μm)

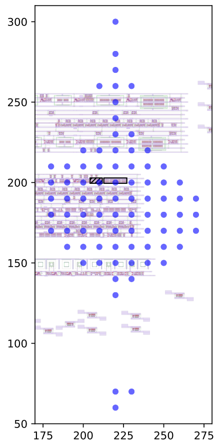
Target BBICS Detection



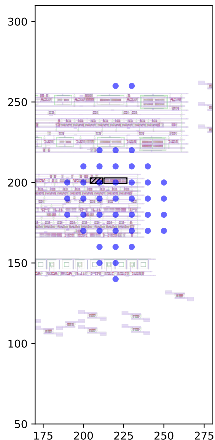
(a) Power = **1.7 W**

Dual-Well Test Structure : 50 ns pulse, 5 μm spot

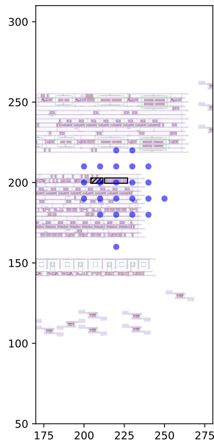
Y position (μm)
X position (μm)
Target
BBICS
Detection



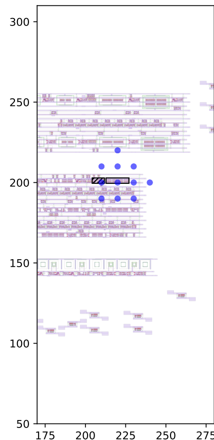
(a) Power = **1.7 W**



(b) Power = 0.7 W



(c) Power = 0.3 W

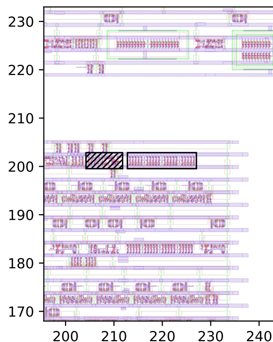


(d) Power = 0.1 W

Dual-Well Test Structure : 30 ps pulse, 1 μm spot

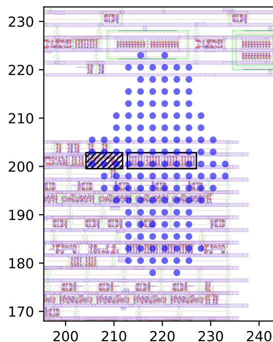
Y position (μm)
X position (μm)

Target BBICS Detection



Dual-Well Test Structure : 30 ps pulse, 1 μm spot

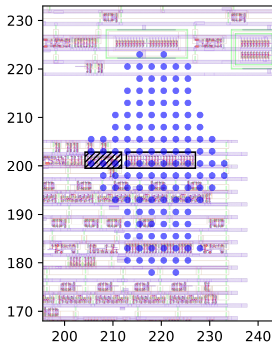
Y position (μm)
X position (μm)
Target
BBICS
Detection



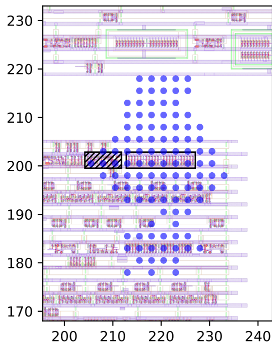
(a) Energy = **2 nJ**

Dual-Well Test Structure : 30 ps pulse, 1 μm spot

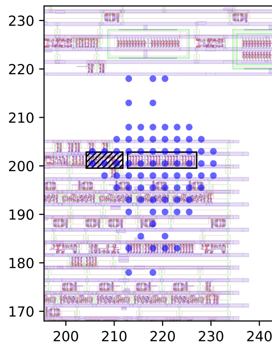
Y position (μm)
X position (μm)
Target
BBICS
Detection



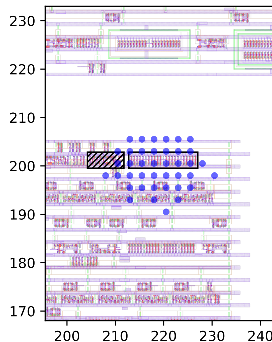
(a) Energy = **2 nJ**



(b) Energy = 1.5 nJ

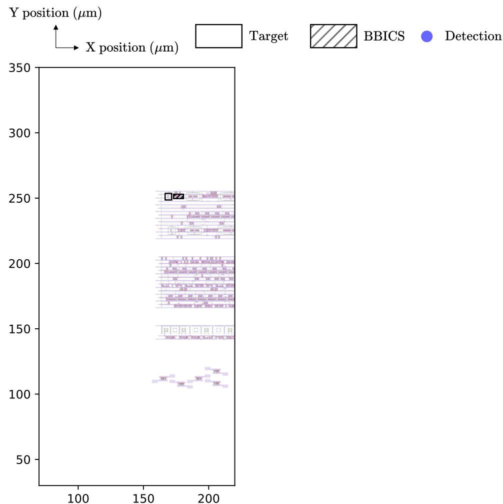


(c) Energy = 1 nJ

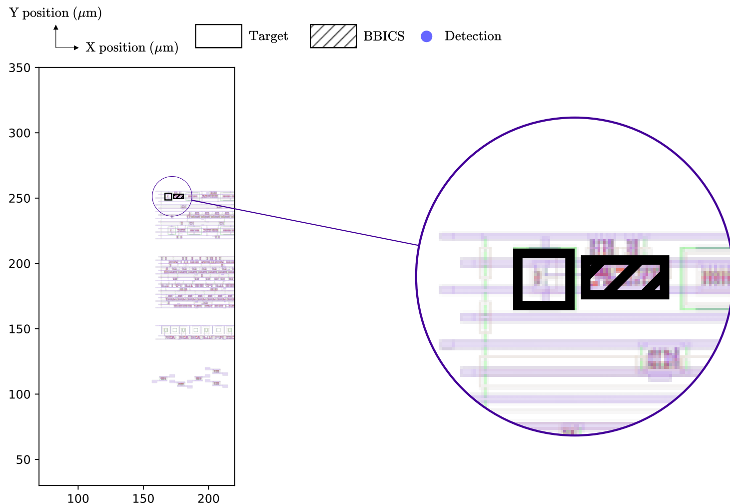


(d) Energy = 0.5 nJ

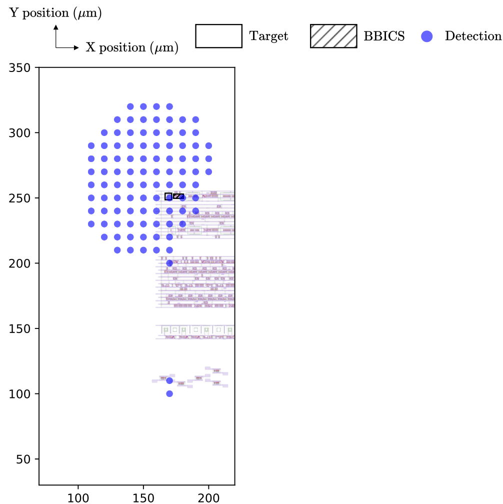
Triple-Well Test Structure : 50 ns pulse, 5 μm spot



Triple-Well Test Structure : 50 ns pulse, 5 μm spot

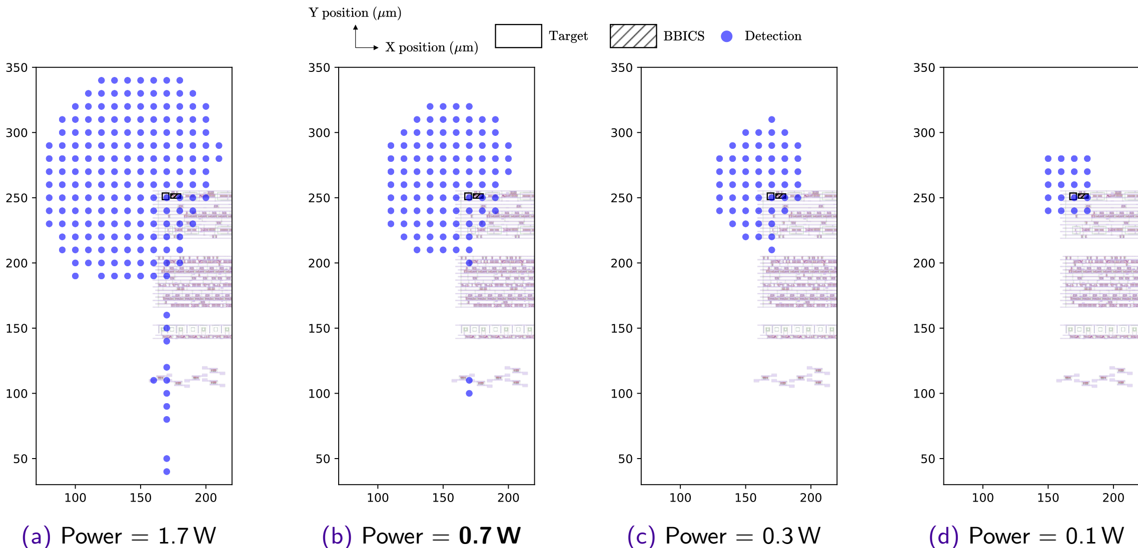


Triple-Well Test Structure : 50 ns pulse, 5 μm spot



(b) Power = **0.7 W**

Triple-Well Test Structure : 50 ns pulse, 5 μm spot



(a) Power = 1.7 W (b) Power = **0.7 W** (c) Power = 0.3 W (d) Power = 0.1 W

Triple-Well Test Structure : 30 ps pulse, 1 μm spot

Y position (μm)
X position (μm)

Target | BBICS | Detection

280
260
240
220
200

150 160 170 180 190

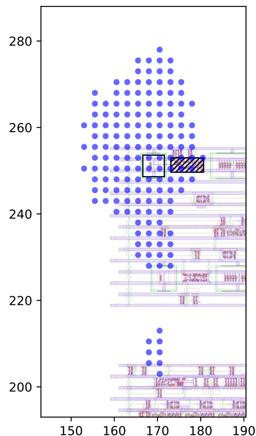
Triple-Well Test Structure : 30 ps pulse, 1 μm spot

Y position (μm)
X position (μm)
Target
BBICS
Detection

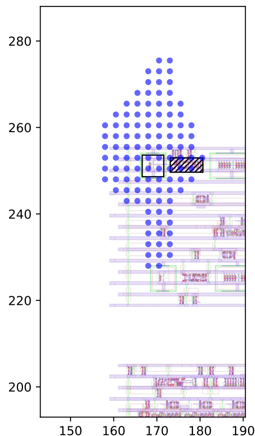
280
260
240
220
200
150 160 170 180 190

(c) Energy = **1 nJ**

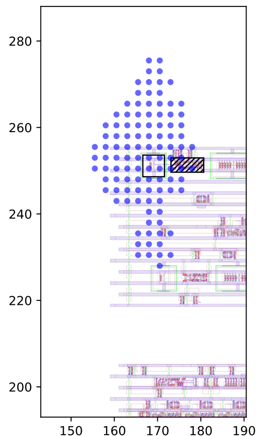
Triple-Well Test Structure : 30 ps pulse, 1 μm spot



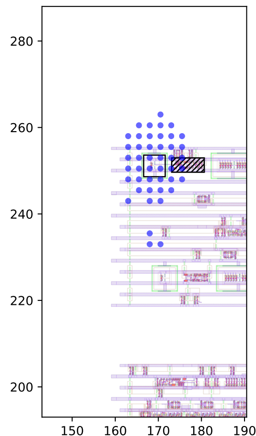
(a) Energy = 2 nJ



(b) Energy = 1.5 nJ



(c) Energy = **1 nJ**



(d) Energy = 0.5 nJ

SYNTHESIS

Sensor area	$22\ \mu m^2$			
Test structure	Dual-Well		Triple-Well	
Target area	$40\ \mu m^2$		$25\ \mu m^2$	
Pulse duration	50 ns	30 ps	50 ns	30 ps
Spot diameter	5 μm	1 μm	5 μm	1 μm
Detection area at fault threshold	$7{,}000\ \mu m^2$	$819\ \mu m^2$	$9{,}500\ \mu m^2$	$638\ \mu m^2$

For every tested parameters:

Target area $\subset$ BBICS Detection area

The BBICS efficiently monitors Triple-Well CMOS logic and Picosecond LFI !

OUTLINE

- BBICS Principle
- BBICS Experimental State-of-the-Art
- Experimental Methodology & Setup
- Experimental Assessment
- Conclusion

Experimental assessment of BBICS LFI monitoring capabilities was provided

Reference	Champeix *et al.*	Borrel *et al.*	Matsuda *et al.*	**This Work**
Technology	90 nm	90 nm	180 nm	**65 nm**
Target	Dual-Well logic	Dual-Well logic Triple-Well logic	Dual-Well AES core	Dual-Well logic Triple-Well logic
Laser pulse duration	200-50 ns	long μs to short ns	60 ns	50 ns and **30 ps**

Study of **BBICS detection area** at parameters associated to logic **fault threshold**...

- **Confirmed** BBICS efficiency in monitoring...
  - 65 nm Dual-Well logic against nanosecond-range pulses
- **Ascertained** BBICS efficiency in monitoring...
  - 65 nm Dual-Well logic against picosecond-range pulses
  - 65 nm Triple-Well logic against nanosecond-range pulses
  - 65 nm Triple-Well logic against picosecond-range pulses

Experimental assessment of BBICS LFI monitoring capabilities was provided

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  - 65 nm Triple-Well logic against picosecond-range pulses

Leverage experimental data for integration ?

CONTACT

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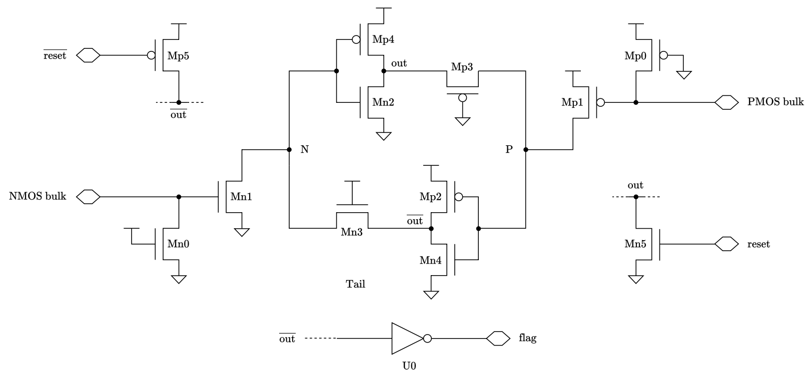
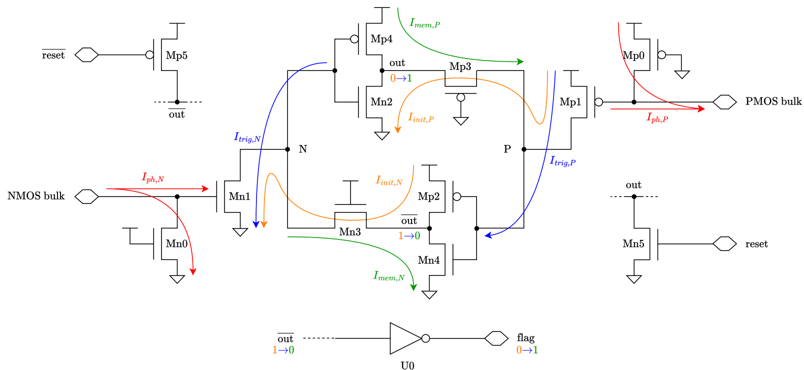
APPENDIX



APPENDIX



APPENDIX